Solar Car Final Report

ENEL372 S2 2025

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Abstract

This project designed, simulated, and built a DC–DC buck converter to power a model solar car directly from a 10 W solar panel. Using a TL494 controller, IPP034N03L MOSFET, and hand-wound RM8 inductor, the converter efficiently regulated voltage to maintain maximum power point operation. The system operated in continuous conduction at 51.3 kHz, closely matching design expectations. PCB implementation reduced noise and improved stability compared with breadboard testing. Results confirmed stable performance and effective power delivery to the motor, demonstrating practical application of switching power electronics and renewable energy integration. Possible improvements included refining the control response, reducing output ripple, and improving the precision of the maximum-power-point adjustment.

The learning outcomes of this project were to demonstrate the practical application and challenges of DC–DC power conversion in renewable energy systems. In a solar-powered car, the supply voltage changes depending on the light intensity and motor load. Without controlling the voltage, the motor could have troubles starting, slow down under load, or waste power. By designing and building a buck converter from first principles, experience was gained in switching power electronics, component selection, efficiency optimization, simulation, and PCB design. All of which are important skills for future work in industry.

Contents

Introduction

This project report outlines the design, simulation, and construction of a DC-DC buck converter to power a model solar car. The car consists of a solar panel mounted on an aluminum chassis with a DC motor, gearbox, and servo. The purpose of the buck converter was to efficiently regulate the variable output from a 10W solar panel to drive the DC motor, so then the car could start and operate solely under solar power without auxiliary batteries.

The project specifications required the use of a buck converter circuit controlled by a TL494 pulse-width modulation (PWM) chip. The design had to include an N-channel MOSFET (IPP034N03L) and a Schottky diode (SB240S) for efficient switching. The inductor core was specified as an RM8 type, which must be designed and hand-wound as part of the project. The total capacitance in the circuit must not exceed 350 µF.

This report details the design, build, and performance of the buck converter, linking theoretical design choices to experimental results. It explains the circuit design process and component selection, presents key simulation and experimental results, and discusses how the converter performed once constructed. It concludes by identifying the limitations of the converter, and potential improvements that could be made for future iterations.

1. Methodology

1.1. Buck converter

To start the analysis, a basic buck converter schematic was chosen from the lecture notes, shown in Figure 1. This follows the governing equation described in (1).

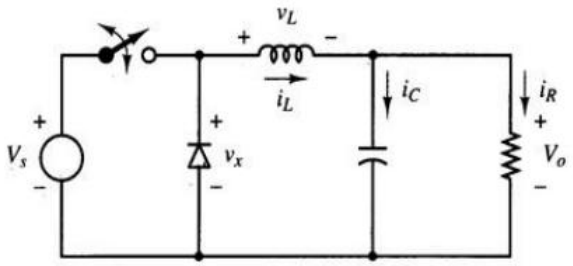


Figure 1: Buck converter schematic

$$V_O = DV_s \tag{1}$$

Next, the discontinuous current in the inductor was considered. From the lecture notes, the minimum operating threshold is given in equation (2). Where I_O is the current over the load (corresponding to i_R in Figure 1), and Δi_L is the ripple current in the inductor.

$$I_O > \frac{\Delta i_L}{2} \tag{2}$$

It was decided that the operating point should be far away from this threshold. An initial guess was chosen, setting I_O to be 30% of Δi_L. This is shown in equation (3).

$$0.3I_O = \Delta i_L \tag{3}$$

Once this relationship was determined, the sizing equations for the inductor and output and capacitors were derived, shown in equations (4) and (5). The details of these derivations are shown in Appendix B. It was determined that a bulk input capacitor was needed to filter out fluctuations from the solar panel and an equation describing this, (6), was found.

$$L = \frac{V_O(1-D)}{0.3I_O f_s} \tag{4}$$

$$C_{out} = \frac{0.3I_O D}{f_s \Delta V_O} \tag{5}$$

$$C_{in} = \frac{I_O}{4f_s \Delta V_s} \tag{6}$$

Assuming that $V_{in} = 15V$ and a worst-case duty cycle, $D = 0.5$, solving equation (1) gives a value of $V_O = 7.5V$. It was assumed that $I_O = 2.5A$, and f_s was chosen to be $50kHz$. The output voltage ripple, ΔV_O, was chosen to be 1% or $0.075V$. Similarly, the source voltage ripple was assumed to be 1% or $0.15V$. These values were substituted into equations (4), (5) and (6). This gave $L = 100\mu H$, $C_{out} = 100\mu F$ and $C_{in} = 83\mu F$.

Through simulation in LTSpice, plots shown in Appendix F, it was found that increasing the inductor to $200\mu H$ decreased the inductor current ripple from $\sim 1V$ to $\sim 0.5V$, and decreased the output voltage ripple. It was decided that these benefits outweighed the slightly smaller efficiency and switching speed the increased number of windings and inductance gives.

1.2. Inductor construction

Once the size of the inductor was finalized, it was physically constructed using the provided RM8i ferrite core and $0.5mm$ gauge copper wire. Using equation (7) from the lecture notes, it was calculated that 31 turns would be sufficient. Working is provided in Appendix C.

$$NA_{min} = \frac{Li_{max}}{B_{max}} \tag{7}$$

It was determined that the reluctance from the ferrite core was not sufficient, and an airgap was designed from equation (8) which yielded a gap of $0.167mm$, working provided in Appendix C.

$$l_{airgap} = \frac{N^2 \mu_o \mu_r}{2L} \tag{8}$$

There was K250 tape readily available which had a thickness of $0.064mm$. Three layers yielded a thickness of $0.192mm$ which was acceptable. Note that although the material used for the gap is not air, it is a non-magnetic insulating tape and thus the relative permeability, μ_r, is roughly equal to one which is a good approximation to the relative permeability of air. Once these values were finalized, the wire was wound around the core, the tape placed between the two inductor core halves and the housing was wrapped in electrical tape to hold it together. The result is shown in Figure 2.

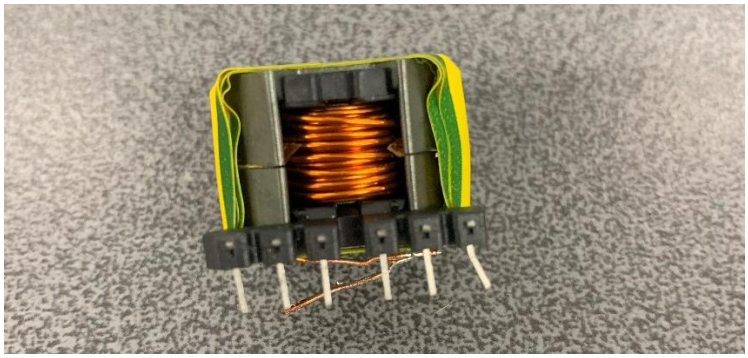


Figure 2: Constructed Inductor

The inductance was measured by connecting the leads of the windings to a Rohde & Schwarz LCR Meter 2 which read $208\mu H$ which was only 3.85% larger than the desired value. This was deemed acceptable for this application.

1.3. Controller

It was decided that the switching functionality of the buck converter was to be achieved with an IPP034 MOSFET. This was to be controlled by the output of a TL494 chip which can provide a modulated duty cycle. For initial circuit simulation and testing, an 'open loop' control system was implemented. This is shown in the LTSpice simulation circuit shown in Appendix F. In this system, the 5V reference voltage generated by the TL494 was fed through a voltage divider into the feedback pin, creating a constant 50% duty cycle.

Once the basic functionality of the buck converter, TL494 and MOSFET were validated through the open loop control system, it was decided that a closed loop system should be implemented to keep the solar panel operating at its maximum power point. It was determined that this maximum power point varied from $14 - 16\text{V}$ based on the light conditions. To ensure the circuit operated at this maximum point, wherever it happened to be, V_{solar} was passed through a variable voltage divider, which stepped down the source voltage to 5V. This was then fed into $\text{V}_{\text{in}-}$, the inverting input of the first op-amp comparator built into the TL494 (connections seen between Figures 3 and 4). This voltage was compared with the 5V reference generated by the TL494 by tracing this output to $\text{V}_{\text{in}+}$, the non-inverting input of the comparator. Once these are equal, the duty cycle stays constant. If $\text{V}_{\text{in}-}$ drifts above 5V from the circuit drawing too high a voltage from the solar panel, the duty cycle will decrease to bring the voltage draw down. Similarly, if $\text{V}_{\text{in}-}$ drops below 5V, the duty cycle will increase to increase the voltage draw, always keeping the voltage draw the maximum power point. However, this maximum point changes with the light conditions day-to-day, to account for this, R_2 of the voltage divider was chosen to be a potentiometer so the maximum power voltage could be fine-tuned day-to-day.

However, the circuit just described would produce almost instant changes, which would lead to rapid changes in duty cycle, potentially creating oscillations and undesired behavior. To slow down the control response speed, integral control was added in the form of a capacitor between $\text{V}_{\text{feedback}}$ and $\text{V}_{\text{in}-}$. This circuit schematic is shown in Figure 3, with its interface with the TL494 chip shown in Figure 4. A full circuit schematic is included in Appendix A. Note that several 0Ω resistors were included to allow the circuit to easily be redesigned if necessary.

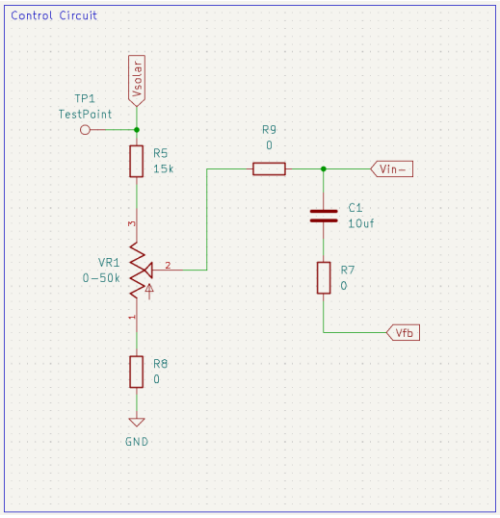


Figure 3: Control circuit

The changes in the suns power happens roughly with a period of 500ms; the control system should have stabilized before the conditions change again. Also, the racetrack is slightly rough, which causes high-frequency bounces roughly 10ms in period, which the control system should not react to. Thus, the time constant of this circuit, given by equation (9), was chosen to be 100ms.

$$\tau = RC \tag{8}$$

It was determined that the capacitor creating this time constant should be ceramic, as electrolytic capacitors have a slow response and can have significant variations from their nominal values. The largest ceramic capacitor available was $10\mu\text{F}$. With this restriction in place on the size of the capacitance and total resistance, calculations were carried out, shown in Appendix D. R_1 was calculated to be $14.3\text{k}\Omega$ and was rounded up to the nearest available size of $15\text{k}\Omega$. R_2 was found to be $33.3\text{k}\Omega$ and a $50\text{k}\Omega$ potentiometer was chosen to accommodate this.

The switching frequency, f_s was chosen to be 50kHz. From the TL494 datasheet, the values of C_T and R_T were chosen to be 10nF and $2.2\text{k}\Omega$, to select this frequency. The TL494 control circuit schematic is shown in Figure 4.

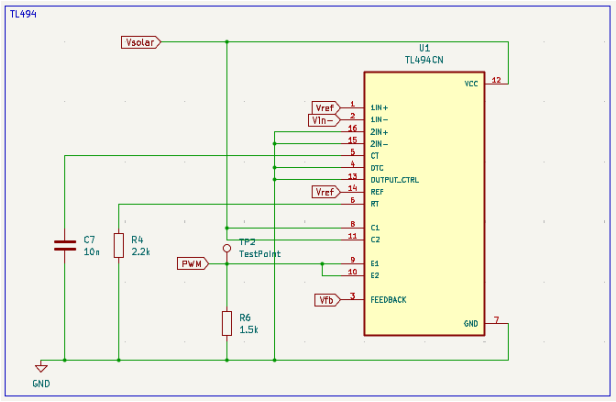


Figure 4: TL494 connection schematic

1.4. BJT driver and switching

The switching MOSFET was placed on the low side of the buck circuit, shown in Figure 5. If it was positioned on high side (the arrangement shown in Figure 1), the switching voltage V_{gs} would have to be $\sim 10\text{V}$ higher than the source voltage which is unfeasible without external power (or a boost converter!). On the low side, V_{gs} only must be $\sim 10\text{V}$ greater than ground, which is easily handled by supplying V_{gs} from V_{solar}.

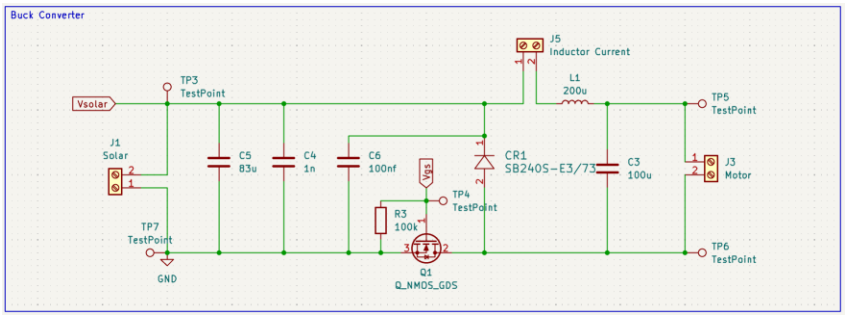


Figure 5: Buck converter schematic

Through simulating the circuit in LTSpice, it was found that the current supplied from the pins of the TL494 wasn't large enough to fully saturate the MOSFET. It was decided that a BJT driver was necessary to amplify the TL494 PWM current. This circuit is shown in Figure 6.

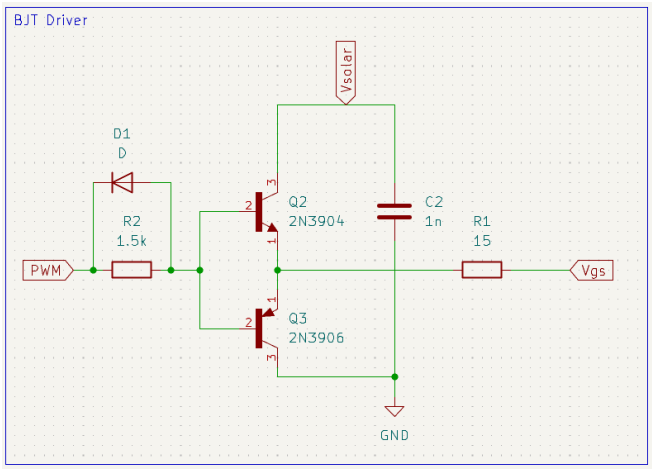


Figure 6: BJT Driver

As seen by comparing Figures 4, 5 and 6 (full circuit schematic supplied in Appendix A), it is seen that the PWM pin from E1 & E2 are fed through the BJT driver to V_{gs}, the gate of the MOSFET controlling the switching of the buck converter. When the PWM pin outputs a high signal, V_{solar} is connected through Q_2 and the current limiting resistor, R_1, to V_{gs}. When the pin outputs a low signal, V_{gs} is connected to ground through R_1 and Q_3. Calculations for R_1, R_2 and R_6 (shown in Figure 4 and Appendix A), are shown in Appendix E. A $1nF$ electrolytic capacitor, C_2, was added to act as a path to ground for high frequencies introduced to the power source caused by the fast switching of Q_2 and Q_3.

1.5. Circuit improvements

After the main components and functions had been designed, several circuit improvements were implemented. First, a $1nF$ ceramic capacitor, C_4, was added in parallel with the solar panel and the input capacitor. This was done to remove high-frequency, low voltage noise from the circuit, as although the bulk input capacitor (C_5 from Figure 5 or Appendix A) filters out low-frequency high voltage, it cannot remove higher frequencies. This is shown in Figure 7.

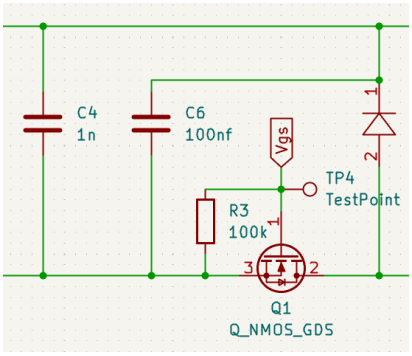


Figure 7: Circuit improvements

A second ceramic capacitor, C_6, was added to reduce the effects of the inductive loop created by high $\frac{di}{dt}$ going through Q_1, the diode and C_4 by proving a path to ground for high frequency signals.

1.6. PCB

Once the circuit schematic was finalized, a PCB was designed, shown in Figure 8.

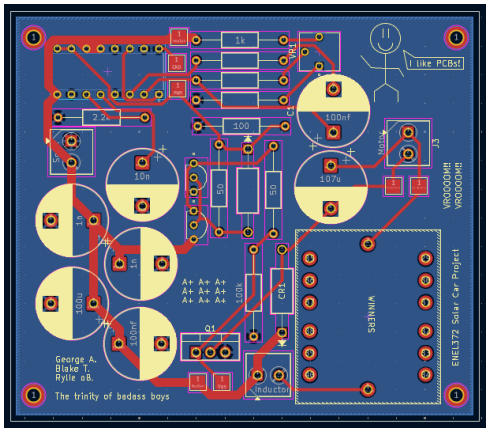


Figure 8: PCB Design

A ground plane was constructed to reduce the return current path for signal and high $\frac{di}{dt}$ traces. Sharp corners on all traces were minimized to reduce them acting as radiating antennas. The power traces were made to be 0.5mm thick to minimize current density, resistance and stray inductance. Where possible, the capacitors were placed as close as possible to the source to reduce stray inductance from high frequency signals and decrease the resistance.

2. Results

The PCB board was constructed. The result is shown in Figure 9.

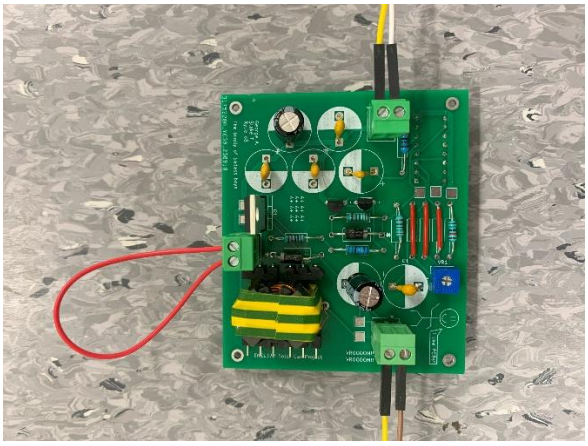


Figure 9: Assembled PCB board

A problem was encountered where the TL494 footprint was accidently flipped to the back side of the board, seen in the top right corner of Figure 9. This was identified by a significant amount of current draw and production of heat when the circuit was assembled. A simple solution was found to solder the chip onto the back of a new board.

The measured gate-source voltage, shown in Figure 10, mirrors the values from the simulated LTspice data, (shown in Appendix F). This confirms the accuracy of the model and the reliability of the circuit's behavior. This shows a peak-to-peak voltage of $14.4V$ which is similar to the simulated V_{gs}.

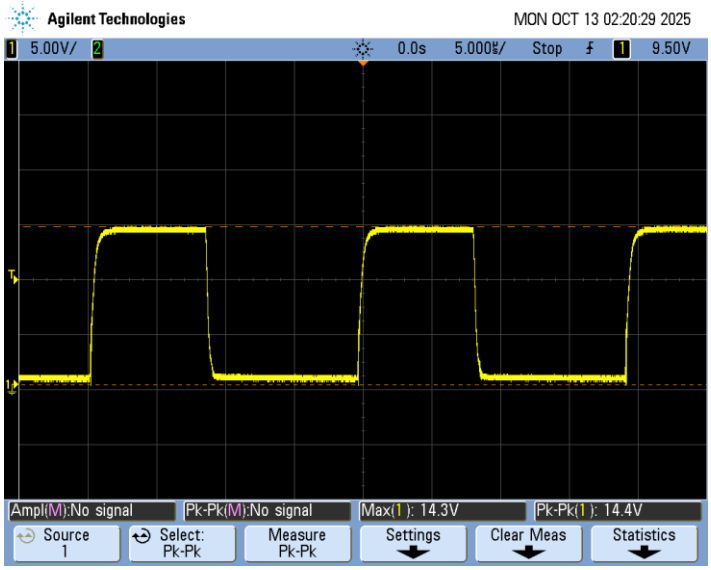


Figure 10: MOSFET Gate Source Voltage

The drain source voltage, shown in Figure 11, shows a clean PWM signal similar of the gate source voltage. The switching frequency is seen to be 51.3kHz which is very close to the chosen frequency of 50kHz. The slight discrepancy can be explained through inaccuracies introduced through large component tolerances for $\mathrm{C_T}$ and $\mathrm{R_T}$. The voltage rise and fall is created by capacitance on the $\mathrm{V_{gs}}$ pin, and the current through R_1 (current limiting resistor into V_{gate} shown in Appendix A).

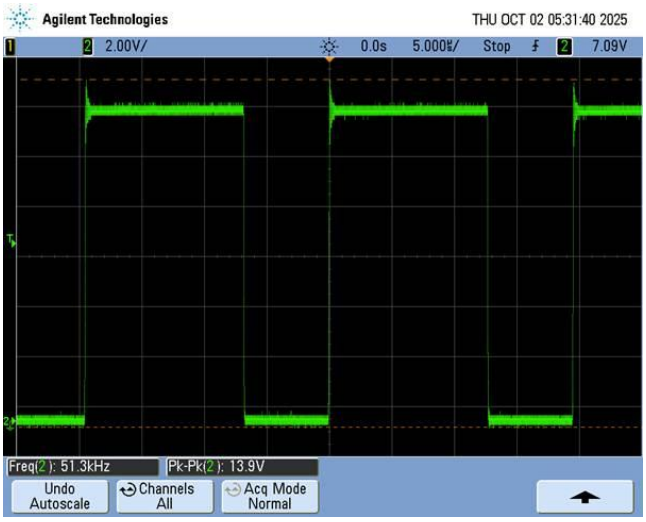


Figure 11: MOSFET Drain Source Voltage

This indicates that the BJT driver is supplying enough current to saturate the MOSFET correctly and voltage is be connected from drain to source. The drain source voltage mirrors the simulated LTspice data (shown in appendix F). The spike from the rise is caused by the inductive loops of the circuit. When there is high current change when the MOSFET is saturated, these loops create a voltage spike which is added onto the PWM waveform, as seen in Figure 11. To reduce the spike from the rise, the inductive loops could be minimized.

The inductor current waveform, shown in Figure 12, remains continuous and exhibits approximately linear behavior similar to an ideal buck converter. This linearity results in a proportional relationship between the converter's gain and the duty cycle, which ensures smooth energy transfer and stable operation.

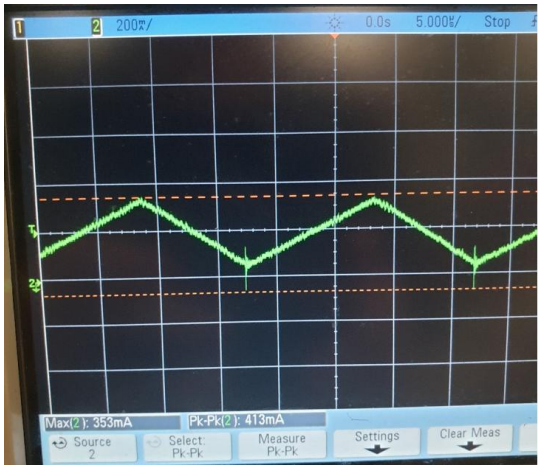


Figure 12: Inductor Current

The input voltage, shown in Figure 13, shows a small voltage ripple along with voltage spikes. The voltage spikes observed are primarily caused by electrical noise and high transients when the switch is turned on. Visually, the voltage ripple, ignoring the spikes, looks close to the intended voltage ripple of $0.15V$. This indicates the

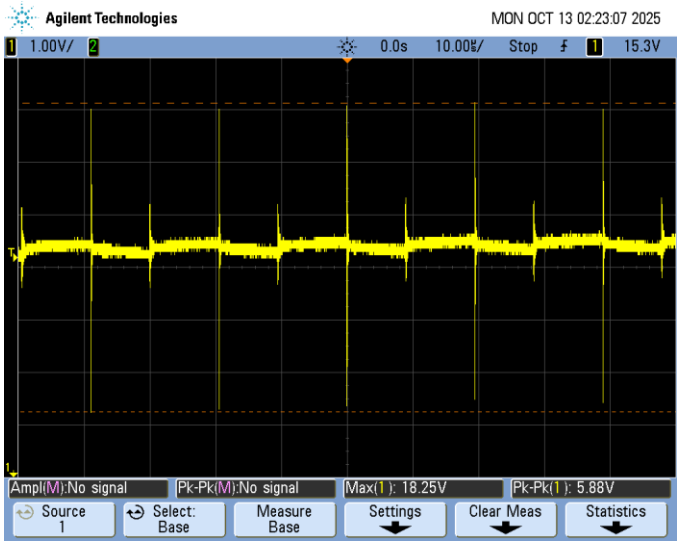


Figure 13: Input Voltage

The voltage ripple on the output was then measured by probing 2 points on each side of the motor while referencing the supply voltage ground. The difference between these two signals was taken to obtain the voltage ripple, shown in Figure 14. The voltage ripple was designed to be $0.075V$ as seen in Appendix B, and the recorded peak to peak was $1.09V$. This is likely due to voltage spikes which are caused by electrical noise originating from the motor load. When visually inspecting the waveform, the actual ripple is closer to the expected value. Another reason for the differences in voltage ripple could be that the output capacitor was designed with a 3 Ohm resistive load, not the exact resistive load of the motor. Additionally, the loops in the motor windings create an inductive load which has small but unexpected effects on the current.

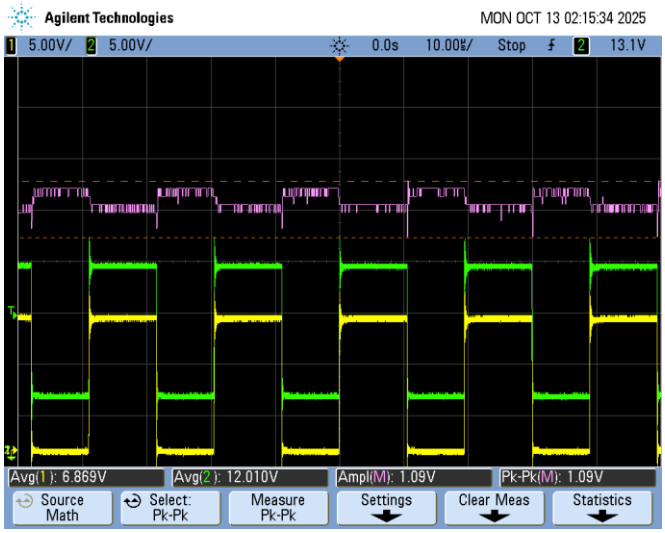


Figure 14: Output Voltage Ripple

3. Discussion

The converter successfully generated a stable output voltage and current sufficient to power the DC motor directly from the solar panel. The integral control loop maintained the operating voltage near the maximum power point under changing light and load conditions, confirming that the closed-loop design worked as intended. The system handled high torque demands during startup and achieved steady-state operation once the solar car was in motion. The converter addressed fluctuations in steady-state operation due to mechanical load variations, ensuring the system's design was stable under both transient and steady-state conditions.

The measured switching frequency of 51.3 kHz from Figure 11 matched the designed 50 kHz, verifying the TL494 timing. The output waveform of the inductor showed continuous-conduction behavior, indicating that the inductor did not saturate.

The solar car used only integral control. This provided stable operation with the time constant slowly ramping up. However, the integral control responded slowly to step changes in light or motor load. While integral control maintained zero steady-state error, it introduced lag during transients, leading to slower voltage recovery after sudden changes in light or motor torque. Adding a proportional term (PI control) by including a resistor before the capacitor in the integral control circuit would have allowed the converter to respond faster during the solar car demonstration. This proportional term would have increased the control loop bandwidth and improved transient response, allowing faster voltage recovery while maintaining steady-state accuracy.

A potentiometer in the voltage divider was used for tuning the maximum power point (MPP) each day, allowing the panel to operate efficiently under different lighting conditions. However, because the adjustment range was wide, small changes in the potentiometer position caused large variations in the reference voltage, making the MPP setting sensitive and difficult to reproduce. Narrowing the resistor range in the divider would have improved fine control and repeatability, making day-to-day tuning more precise and less dependent on small mechanical adjustments.

Moving from a breadboard to a PCB design reduced unstable behavior predominantly caused by inductive loops. By moving to a PCB, the shorter trace lengths and reduced inductive loops stopped the gate-source voltage from rapidly switching on transitioning low to high, which was causing unstable behavior in the bread board setup. The PCB also provided a solid ground plane and shorter high-current paths, reducing parasitic loop area and electromagnetic interference. This improved waveform clarity and reduced switching noise. One problem we had was having the TL494 trace on the back of the PCB. This did not cause any issues with the efficiency of the converter. However, having the TL494 on the top of the PCB with all other components would have made the PCB easier to debug, trouble shoot, and look better visually.

An area for improvement in the design process was the selection and implementation of capacitor footprints on the PCB. Space could be saved by not using electrolytic capacitor footprints for ceramic capacitors.

No capacitor was placed across the motor terminals since the motor operating frequency was much lower than the converter’s 51.3 kHz switching frequency, so harmonic interference was minimal. However, the brushed DC motor still generated high-frequency commutation noise that coupled back into the circuit as small voltage spikes. Adding a small 100 nF ceramic capacitor across the motor terminals would have helped suppress this noise and improve output voltage smoothness.

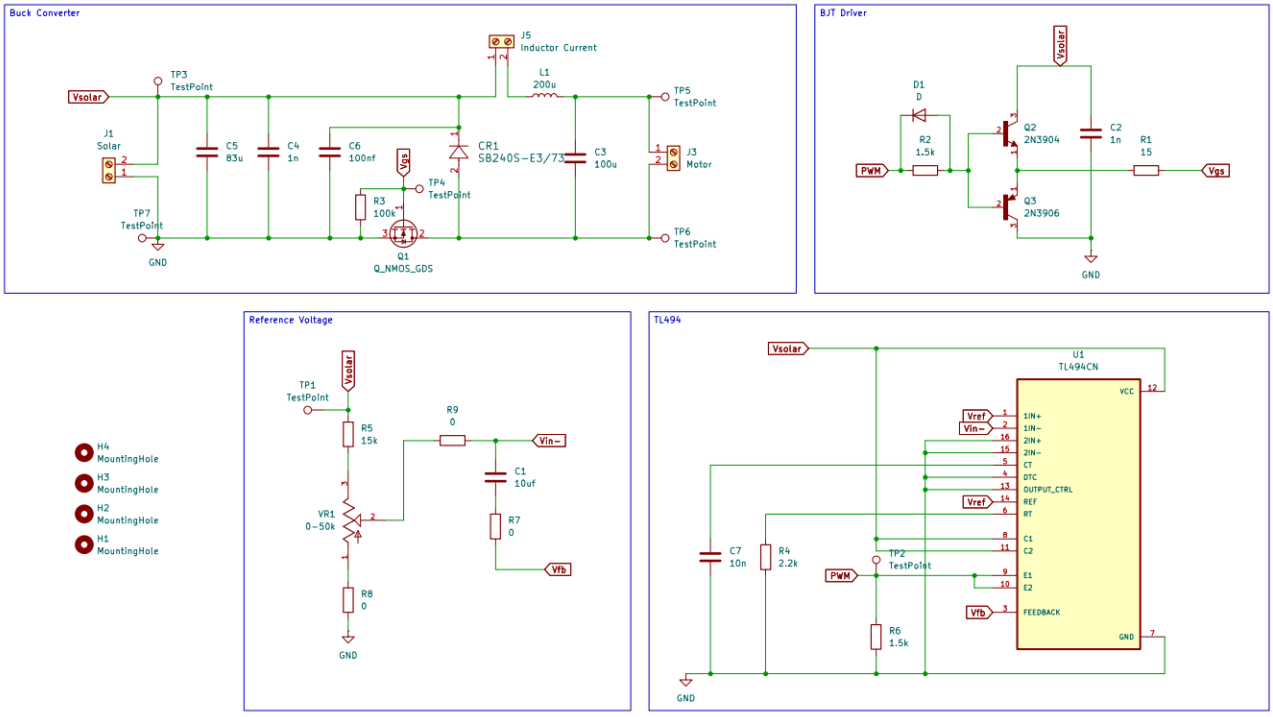
4. Conclusion

The circuit met its design objectives, delivering stable and efficient power from a solar panel to a DC motor under dynamic load. Results closely matched expectations and confirmed continuous conduction mode operation. Transitioning from breadboard to PCB significantly improved signal integrity by minimizing parasitic inductance.

Overall, the converter met its design goal of regulating the solar panel output to power the DC motor smoothly. The control system worked well, the PCB design was a big improvement, and the circuit performed reliably. Future versions could focus on refining the control response, improving ripple performance, and testing the alternative gate driver configuration to get even better efficiency and stability.

5. Appendices

5.1. Appendix A



Full circuit schematic

5.2. Appendix B

Inductor sizing

Operating at the threshold:

$$I_O = \frac{\Delta i_L}{2} = 0.5\,\Delta i_L$$

From this we can derive the minimum inductor size:

$$\Delta i_{L\,open} = -\frac{V_O(1-D)}{Lf_S}$$

$$2I_O > |\Delta i_{L,open}|$$

$$I_O > \frac{V_O(1-D)}{2Lf_S}$$

$$L > \frac{V_O(1-D)}{2I_O f_S}$$

Using a set threshold with 30% tolerance:

$$0.3\,I_O = \Delta i_L$$

gives us:

$$L = \frac{V_O(1-D)}{0.3 I_O f_S},$$

Substituting,

$V_O = 2.5V$ $\quad I_O = 2.5A$
$D = 1/2$ $\quad f_S = 50\,KHz$

we get

$$L = \frac{2.5\,(1-0.5)}{0.3 \times 2.5 \times 50\times10^3} = 100\mu H$$

we increased this to 200μH later as the simulation showed a large transient current spike, and followed the advice of the lab technicians.

Input capacitor

Using the expression from the lecture notes:

$$C_{in} > \frac{I_O}{4 f_S \Delta V_S}$$

and substituting the same values as before, assuming 1% source ripple,

$$\frac{\Delta V_S}{V_S} = 0.01, \quad \Delta V_S = 0.15\,V$$

$$C_{in} > \frac{2.5}{4\times50\times10^3 \times 0.15} > 83\,\mu F$$

Round up to 100μF for safety.

Output capacitor

assuming that all the voltage ripple from the inductor goes through the output capacitor:

$$\Delta i_L = C\frac{dV}{dt} = C\frac{\Delta V}{\Delta t} = C\frac{\Delta V_O}{\Delta t} = C\frac{f_S \Delta V_O}{D}$$

(output ripple; discrete time; time charging)

Substituting $0.3\,I_O = \Delta i_L$,

$$0.3 I_O = C\frac{f_S \Delta V_O}{D}$$

$$C = \frac{0.3 I_O D}{f_S \Delta V_O}$$

We chose 1% ripple:

$$\frac{\Delta V_{out}}{V_{out}} = 0.01, \quad \Delta V_{out} = 0.075$$

Substituting the same values as before:

$$C = \frac{0.3\times2.5\times0.5}{50\times10^3 \times 0.075} = 100\,\mu F$$

5.3. Appendix C

Inductor Construction

Winding calculations

$$NA_{min} = \frac{L i_{max}}{B_{max}}$$

Assuming $B_{max} = 0.3T$

calcs gave us 100 µH, increase to reduce damage due to transient

$L = 200\mu H$
$i_{max} = 2.5A$
$A_{min} = 55.4 \times 10^{-6}\ m$

$$N = \frac{L\, i_{max}}{B_{max} A_{min}} = \frac{200\times10^{-6} \times 2.5}{0.3 \times 55.4\times10^{-6}} = 30.08 \therefore 31 \text{ turns}$$

airgap reluctance:

$R = \frac{N^2}{L}$ $\quad R\mu_0\mu_r A = 2 l_{airgap}$ $\quad$ assuming μ_r paper = 1

$$2 l_{airgap} = R\mu_0\mu_r A = \frac{N^2\mu_0\mu_r A}{L}$$

$$l_{airgap} = \frac{N^2\mu_0\mu_r A}{2L} =$$

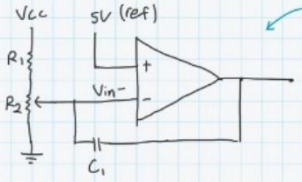
$$l_{airgap} = \frac{31^2 \times 4\pi\times10^{-7} \times 1 \times 55.4\times10^{-6}}{2\times200\times10^{-6}} = 0.167\text{ mm}$$

$\therefore$ 4 250 tape, 0.064 mm/layer $\therefore$ use 3

ended up with 208 µH!

5.4. Appendix D

Feedback (integrator circuit)



Simplifying the schematic to not include zero ohm resistors

Was told that max τ is 500ms, chose τ = 100ms for buffer.

$\tau = RC = 0.1$

Use ceramic capacitor as it is used for control and not bulk energy storage → higher precision but lower values.

Arbitrarily choose $C_{max} = 10\mu F$, can adjust later if needed

So,

$C_{max} = 10\ \mu F$,

$V_{in-} = V_{cc} \frac{R_1}{R_1+R_2}$

$R_T = \frac{\tau}{C} = \frac{0.1}{10\times10^{-6}} = 10000$

$R_T = R_1 // R_2$, $\frac{1}{R_T} = \frac{1}{R_1} + \frac{1}{R_2}$

We designed for Vin=15V, V_{ref} = 5V, so design for V_{in-} = 5V.

$\frac{V_{in-}}{V_{cc}} = \frac{1}{3} = \frac{R_1}{R_1+R_2}$

$\frac{V_{in-}}{V_{cc}} = \frac{R_1}{R_1 + \frac{1}{\left(\frac{1}{10\times10^3} - \frac{1}{R_1}\right)}} = 0.3$

So, to get $\tau = 0.1$, $R_{total} = R_1 // R_2 = 10K\Omega$

$\frac{1}{10\times10^3} = \frac{1}{R_1} + \frac{1}{R_2}$

$\frac{1}{R_1} = \frac{1}{200\times10^3} - \frac{1}{R_2}$

$1 = R_1\left(\frac{1}{200\times10^3} - \frac{1}{R_2}\right)$

$R_2 = \frac{1}{\left(\frac{1}{200\times10^3} - \frac{1}{R_1}\right)}$

Solving for intersection point in desmos:

$R_1 = 14286\ \Omega$,

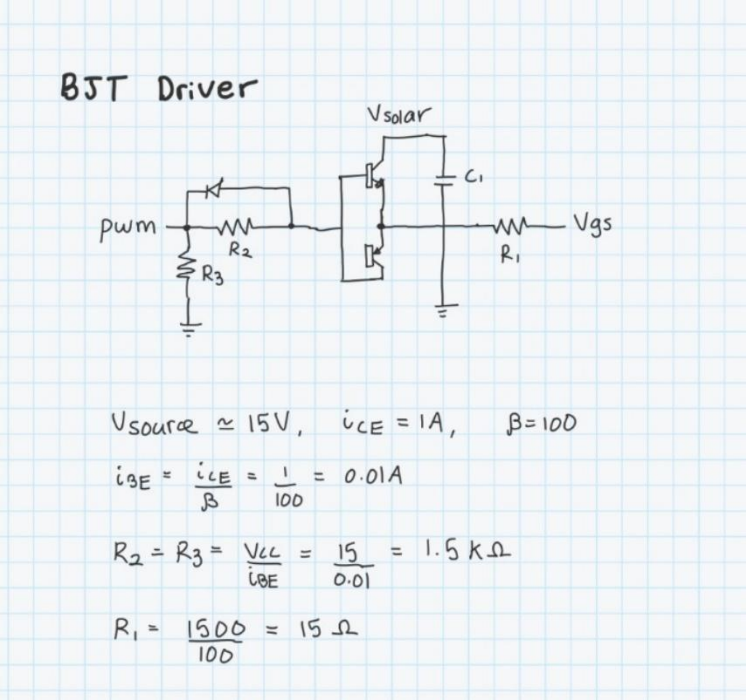
We can then solve for R_2

$\frac{1}{R_T} = \frac{1}{R_1} + \frac{1}{R_2}$

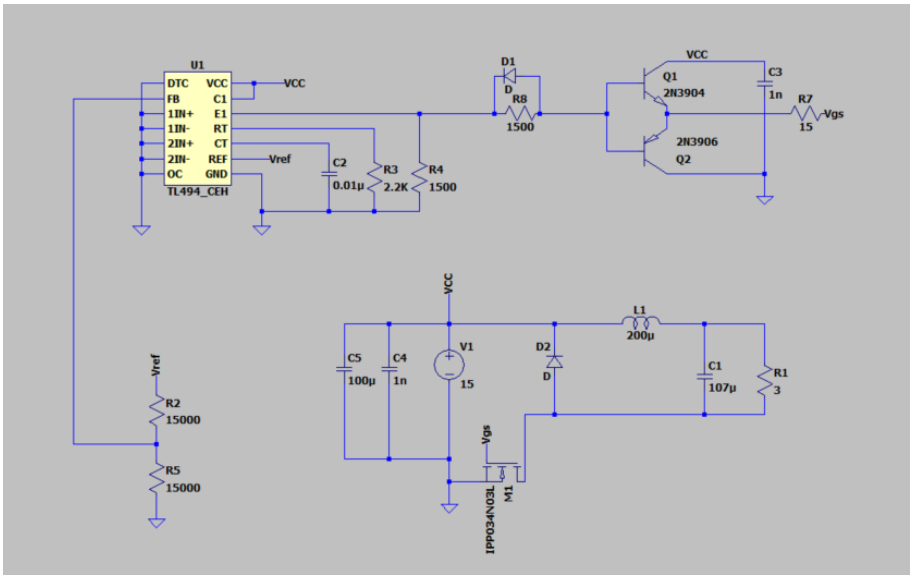
$\frac{1}{16\times10^3} = \frac{1}{14286} + \frac{1}{R_2}$,

$R_2 = 33331\ \Omega$

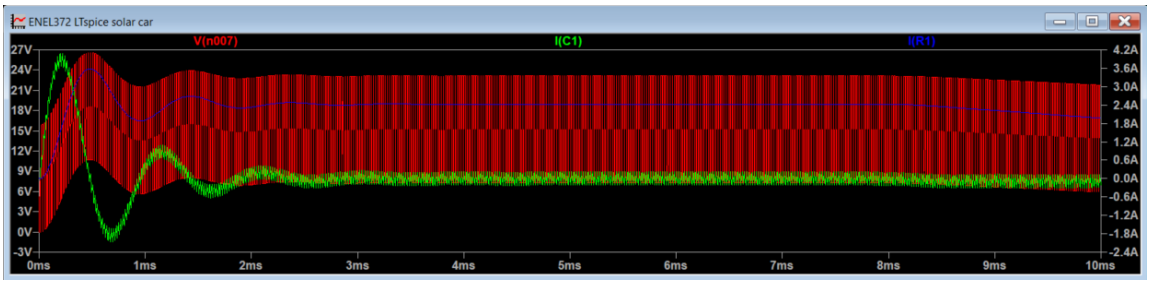
5.5. Appendix E



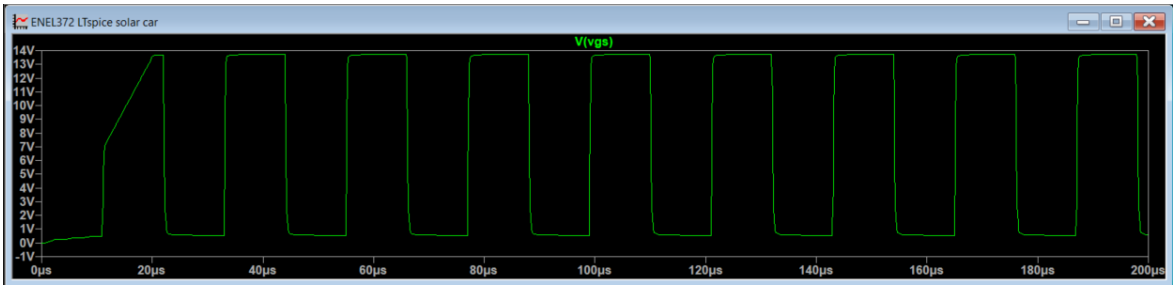
5.6. Appendix F



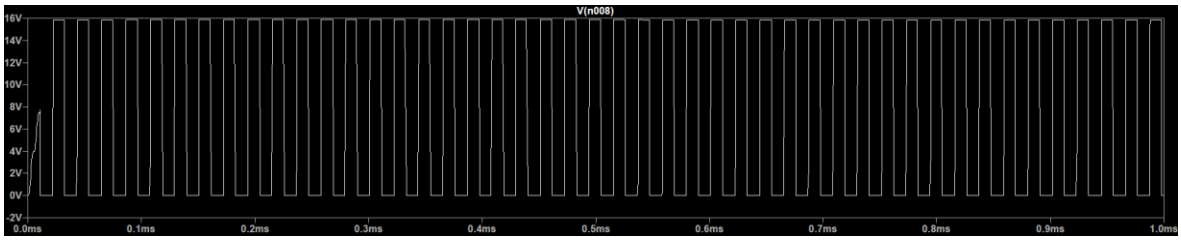
LT Spice schematic used for simulation:



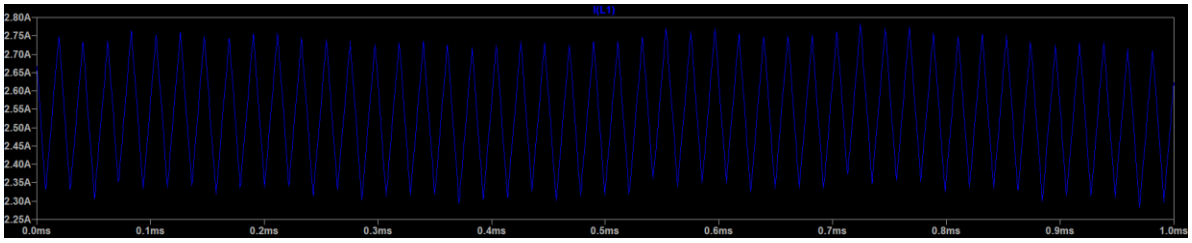
V_{out}, I_c and I_{out} for $L = 200\mu H$ in LTSpice



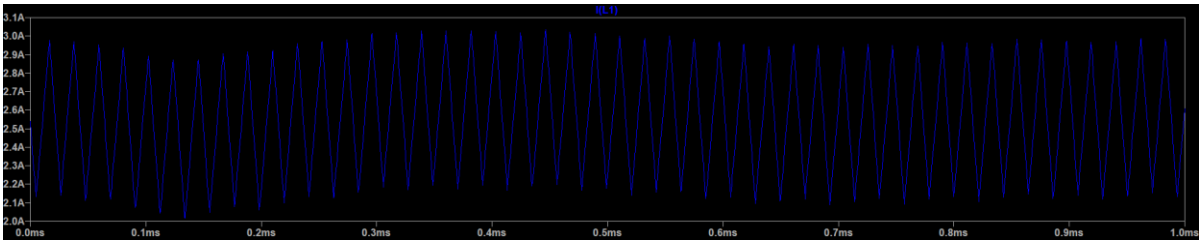
V_{gs} in LTSpice



V_{ds}



I_L @ $200\mu H$



I_L @ $100\mu H$